ABSTRACT OF THE DISCLOSURE

The present invention provides a structure in which a glue layer is formed on an active area and a shallow trench isolation with a glue layer interposed therebetween. A P-type silicon substrate includes the active area partitioned by the shallow trench isolation. An N^+-type semiconductor region is formed in the active area. An interlayer insulation film is formed on the shallow trench isolation and active area, and has an opening to which the shallow trench isolation, active area, and a boundary between them are exposed. A glue layer is formed in the opening. Local interconnect wiring is formed in the opening and electrically connected to the N^+-type semiconductor region through the glue layer. The active area overlaps the shallow trench isolation, and the glue layer has a portion opposed to the N^+-type semiconductor region through the shallow trench isolation underlying the overlap of the active area.